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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/579,385	05/11/2006	Satoru Shiratsuchi	06299/LH	8214

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EXAMINER	
VLAHOS, SOPHIA	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
03/31/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/579,385	SHIRATSUCHI ET AL.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *2* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2006*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-20* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/11/06* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/11/06, 6/6/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Acknowledgment is made of applicant's claim for foreign priority (JP 2004-286548) under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 5/11/06 and 6/06/07 have been considered by the examiner.

3. This application is in condition for allowance except for the following formal matters:

Specification

4. The abstract of the disclosure is objected to because it exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Claim Objections

5. Claim 1, 11 are objected to because of the following informalities:

Claim 1, line 27, recites "a operational amplifier", should be "an operational amplifier"

Claim 11, (page 81, line 6) recites "a operational amplifier", should be "an operational amplifier".

Allowable Subject Matter

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art of the record fails to teach or suggest alone or in combination: A digital signal offset adjusting apparatus comprising: a(n) operational amplifier, a first input end of which is connected to the other end of the first coil, a second input end of which is connected to the direct current voltage generator, an output end of which is connected to another end of the second coil, and which outputs to the output terminal via the other end of the second coil from the output end, the low frequency band of the input digital signal passed to the other end of the first coil input to the first and second input ends and a composite signal obtained by combining the direct current component and the direct current bias voltage output from the direct current voltage generator; and a frequency characteristic compensating circuit connected between a reference electrical potential point and the second input end of the operational amplifier or between the second input end and the output end, the compensating circuit being adopted to compensate for a frequency characteristic so that a gain of the operational amplifier increases with a component having a higher frequency from among the low frequency bands of the input digital signal passed to the other end of the first coil, as recited in claim 1 and in combination with other elements of the claim.

Claims 1-5 are allowed over prior art.

The prior art of the record fails to teach or suggest alone or in combination: A pulse pattern generator comprising: a digital signal offset adjusting apparatus, wherein the digital signal offset adjusting apparatus comprises: a(n) operational amplifier, a first input end of which is connected to the other end of the first coil, a second input end of which is connected to the direct current voltage generator, an output end of which is connected to another end of the second coil, and which outputs to the output terminal via the other end of the second coil from the output end, the low frequency band of the input digital signal passed to the other end of the first coil input to the first and second input ends and a composite signal obtained by combining the direct current component and the direct current bias voltage output from the direct current voltage generator; and a frequency characteristic compensating circuit connected between a reference electrical potential point and the second input end of the operational amplifier or between the second input end and the output end, the compensating circuit being adopted to compensate for a frequency characteristic so that a gain of the operational amplifier increases with a component having a higher frequency from among the low frequency bands of the input digital signal passed to the other end of the first coil, as recited in claim 11 and in combination with other elements of the claim

Claims 11-15 are allowed over prior art.

The prior art of the record fails to teach or suggest alone or in combination: A digital signal offset adjusting apparatus comprising: a first operational amplifier, a first input end of which is connected to the other end of the first coil, a second input end of which is connected to a reference electrical potential point, and which outputs from an output end a first inverted and amplified signal obtained by inverting and amplifying the low frequency band and the direct current component of the input digital signal passed to the other end of the first coil; a second operational amplifier, a first input end of which is connected to the direct current voltage generator, a second input end of which is connected to the reference electrical potential point, and which outputs from an output end a second inverted and amplified signal obtained by inverting and amplifying the direct current bias voltage output from the direct current voltage generator; a third operational amplifier, a first input end of which is connected in common to each of the output ends of the first and second operational amplifiers, a second input end of which is connected to the reference electrical potential point, and which inverts and amplifies a combined signal obtained by combining the first and second inverted and amplified signals and outputs the inverted and amplified signal to the other end of the second coil; and first and second frequency characteristic compensating circuits connected between the reference electrical potential point and each of the first input end of the first and third operational amplifiers or between each of the first input end and the output end of the first and third operational amplifiers, the first and second frequency characteristic compensating circuits being adopted to compensate for a frequency characteristic so that a gain of each of the first and third operational amplifiers increases with a

component having a higher frequency from among the low frequency bands of the input digital signal passed to the other end of the first coil, as recited in claim 6 and in combination with other elements of the claim.

Claims 6-10 are allowed over prior art

The prior art of the record fails to teach or suggest alone or in combination: A pulse pattern generator comprising: a digital signal offset adjusting apparatus, wherein the digital signal offset apparatus comprises: a first operational amplifier, a first input end of which is connected to the other end of the first coil, a second input end of which is connected to a reference electrical potential point, and which outputs from an output end a first inverted and amplified signal obtained by inverting and amplifying the low frequency band and the direct current component of the input digital signal passed to the other end of the first coil; a second operational amplifier, a first input end of which is connected to the direct current voltage generator, a second input end of which is connected to the reference electrical potential point, and which outputs from an output end a second inverted and amplified signal obtained by inverting and amplifying the direct current bias voltage output from the direct current voltage generator; a third operational amplifier, a first input end of which is connected in common to each of the output ends of the first and second operational amplifiers, a second input end of which is connected to the reference electrical potential point, and which inverts and amplifies a combined signal obtained by combining the first and second inverted and amplified

signals and outputs the inverted and amplified signal to the other end of the second coil; and first and second frequency characteristic compensating circuits connected between the reference electrical potential point and each of the first input end of the first and third operational amplifiers or between each of the first input end and the output end of the first and third operational amplifiers, the first and second frequency characteristic compensating circuits being adopted to compensate for a frequency characteristic so that a gain of each of the first and third operational amplifiers increases with a component having a higher frequency from among the low frequency bands of the input digital signal passed to the other end of the first coil, as recited in claim 16 and in combination with other elements of the claim.

Claims 16-20 are allowed over prior art.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 25 USPQ 74, 453 O.G. 213, (Comm'r Pat. 1935).

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McEwan (U.S. 5,883,591)

Saari (U.S. 4,441,080)

Huellwegen (U.S. 4,255,812)

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is (571)272-5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SOPHIA VLAHOS/
Examiner, Art Unit 2611
3/24/2009

/Mohammad H Ghayour/
Supervisory Patent Examiner, Art Unit 2611